Exercise

|  |  |  |
| --- | --- | --- |
| **Decimal** | **Binary** | **Hexadecimal** |
| **2007** |  |  |
|  | **11011** |  |
|  |  | **DFEC** |

Addition:

Subtraction:

Overflow -

Carry -

|  |  |  |  |
| --- | --- | --- | --- |
|  | Signed Magnitude | 2s complement | Unsigned binary |
| Benefits |  |  |  |
| Problems |  |  |  |
| Range |  |  |  |
| Range for b = 4 |  |  |  |

**Logic Gates**

|  |  |  |  |
| --- | --- | --- | --- |
| **Type and Equation** | **Schematic symbol** | **Truth table** | **VHDL** |
| Buffer (BUF) |  | |  |  | | --- | --- | |  |  | |  |  | |  |  | | y <= a; |
| Inverter (INV or NOT) |  | |  |  | | --- | --- | |  |  | |  |  | |  |  | | y <= not a; |
| AND |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | | y <= a and b; |
| OR |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | | y <= a or b; |
| XOR |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | | y <= a xor b; |
| NAND |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | | y <= a nand b; |
| NOR |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | | y <= a nor b; |
| XNOR |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | | y <= a xnor b; |